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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/512,978	02/24/2000	Robert Kerr	MI22-1343	5932

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/512,978	Kerr et al.
Examiner	**Art Unit**
Phat X. Cao	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *May 24, 2002*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *51-62* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *51-60 and 62* is/are rejected.

7) ☒ Claim(s) *61* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Prosecution Application

1. The request filed on 5/24/02 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/512,978 is acceptable and a CPA has been established. An action on the CPA follows.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 51-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno (US. 5,895,939).

With respect to claim 51, Ueno (Fig. 6) discloses an integrated circuit comprising: a semiconductor substrate 63; a diffusion region 65 formed within the substrate, the diffusion region 65 and substrate 63 forming a junction; a conductive line 67 formed over the substrate and diffusion region, a portion of the conductive line 67 over the diffusion region 65 comprising an entirely of the lateral width of the conductive line 67 received directly over the diffusion region; and wherein the junction is configured to be reverse biased to preclude electrical shorting between

the conductive line 67 and the substrate 63 for selected magnitudes of current provided through the conductive line (column 9, lines 65-67 through column 10, lines 1-2).

Ueno does not disclose the conductive line 67 having a generally uniform lateral width. However, it would have been obvious to form the conductive line 67 having a generally uniform lateral width because it has been held that changing in shape of parts of an invention is generally recognized as being within the level of ordinary skill in the art. *In re Dailey*, 357 F. 2d 669, 149 USPQ 47 (CCPA 1966). It appears that these changes produce no functional different and therefore would have been obvious. *In re Woodruff*, 919 F. 2d 1575, 1578, 16 USPQ 2d 1934, 1936 (Fed. Cir. 1990).

With respect to claims 52-54, Ueno's Fig. 6 further discloses the diffusion region 65 comprises two portions disposed outwardly from directly beneath the conductive line, a first portion outward of a first side of the conductive line and a second portion outward of a second side of the conductive line.

4. Claims 51-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batra et al (US. 6,242,781) in view of Wolf (Vol. 3).

With respect to claim 51, Batra (Fig. 10) discloses an integrated circuit comprising: a semiconductor substrate 55; a source diffusion region 16 formed within the substrate, the source diffusion region 16 and substrate 55 forming a junction; a conductive gate line 28 formed over the substrate and diffusion region, the conductive gate line 28 having a generally uniform lateral

width, and a portion of the conductive line 28 over the diffusion region 16 comprising an entirety of the lateral width of the conductive line received directly over the diffusion region.

Batra does not specifically disclose that the diffusion region and substrate forming a reverse biased junction for selected magnitudes of current provided through the conductive line.

However, Wolf teaches the obviousness of using n and p dopants in four different MOSFETs configurations, formation of pn junction and reverse biasing a pn junction of the diffusion region and the substrate by selectively apply magnitudes of voltage provided through the conductive gate line of MOSFET (see Fig. 4-2 on page 137 and related text, on page 136, section 4.1.1). Accordingly, it would have been obvious to form a reverse biased pn junction between the diffusion region and the substrate for selected magnitudes of voltage on current provided through the conductive gate line because according to Wolf, this is a basis operation of a MOS transistor when the transistor is in OFF mode (also see Fig. 4-2 and section 4.1.1).

5. Claims 51-60 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yen (US. 5,965,924) in view of Wolf (Vol. 3).

Yen, in Figs. 3A and 3B, discloses an integrated circuit comprising: a semiconductor substrate 74; a diffusion region 70 formed within the substrate, the diffusion region 70 and substrate 74 forming a junction; a conductive gate line 74 formed over the substrate and the diffusion region; a conductive material 80 made of metal interconnecting the conductive gate line 74 and the diffusion region 70, a portion of the conductive material 80 received directly over the conductive line, and an entirety of the portion of the conductive material 80 received directly over

the diffusion region 70 (see Fig. 3A); wherein the diffusion region 70 comprises at least two portions disposed outwardly from directly beneath the conductive material 80, and comprises a portion disposed outwardly from directly beneath the combined cross sectional area of the conductive material 80 and the conductive line 74.

Yen does not specifically disclose that the diffusion region and substrate forming a reverse biased junction for selected magnitudes of current provided through the conductive line.

However, Wolf teaches the obviousness of using n and p dopants in four different MOSFETs configurations, formation of pn junction and reverse biasing a pn junction of the diffusion region and the substrate by selectively apply magnitudes of voltage provided through the conductive gate line of MOSFET (see Fig. 4-2 on page 137 and related text, on page 136, section 4.1.1). Accordingly, it would have been obvious to form a reverse biased pn junction between the diffusion region and the substrate for selected magnitudes of voltage on current provided through the conductive gate line because according to Wolf, this is a basis operation of a MOS transistor when the transistor is in OFF mode (also see Fig. 4-2 and section 4.1.1).

6. Claims 51-54, 59-60, and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura (US. 5,278,082) in view of Wolf (Vol. 3).

Kawamura (Fig. 1H) discloses an integrated circuit comprising: a semiconductor substrate 1; a diffusion region 10 formed within the substrate, the diffusion region 10 and substrate 1 forming a junction; a conductive gate line 41 formed over the substrate and the diffusion region; a conductive material 300 interconnecting the conductive gate line 41 and the diffusion region 10, a

portion of the conductive material 300 received directly over the conductive gate line, and an entirety of the portion of the conductive material 300 received directly over the diffusion region; and wherein the diffusion region 10 comprises a portion disposed outwardly from directly beneath the combined cross-sectional area of the conductive material 300 and the conductive line 41.

Kawamura does not specifically disclose that the diffusion region and substrate forming a reversed biased junction for selected magnitudes of current provided through the conductive line.

However, Wolf teaches the obviousness of using n and p dopants in four different MOSFETs configurations, formation of pn junction and reverse biasing a pn junction of the diffusion region and the substrate by selectively apply magnitudes of voltage provided through the conductive gate line of MOSFET (see Fig. 4-2 on page 137 and related text, on page 136, section 4.1.1). Accordingly, it would have been obvious to form a reverse biased pn junction between the diffusion region and the substrate for selected magnitudes of voltage on current provided through the conductive gate line because according to Wolf, this is a basis operation of a MOS transistor when the transistor is in OFF mode (also see Fig. 4-2 and section 4.1.1).

Allowable Subject Matter

7. Claim 61 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to the claimed invention have been considered but are moot in view of the new ground(s) of rejection.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917. The Examiner can normally be reached on Monday through Thursday. If attempts to reach the Examiner by telephone are unsuccessfully, the Examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. Group 2800 fax number is (703) 308-7722 or (703) 308-7724.

PHAT X. CAO
PRIMARY EXAMINER

PC
June 30, 2002